

WHAT IS CLAIMED IS:

- 1 1. A method for fabricating a metal oxide semiconductor field effect transistor
- 2 (MOSFET) comprising the steps of:
 - 3 providing a substrate having spaced apart source and drain regions on the
 - 4 substrate with the space between the source and drain regions defining a channel region;
 - 5 forming a dielectric layer peripherally about the drain portion to completely
 - 6 surround the drain region and in contact with the source region to fill the channel region,
 - 7 wherein the area of the dielectric layer in the channel region between the drain and source
 - 8 regions is variable in length; and,
 - 9 forming a gate electrode layer on at least a portion of the dielectric layer in the
 - 10 channel region.
- 1 2. The method of Claim 1, wherein the substrate is a layer of mono-crystalline
- 2 silicon, the dielectric layer is silicon dioxide and the gate electrode layer is poly-crystalline
- 3 silicon.
- 1 3. The method of Claim 1, wherein a width-length ratio of the transistor is less
- 2 than or equal to unity
- 1 4. The method of Claim 2, wherein a width-length ratio of the transistor is less
- 2 than or equal to unity.
- 1 5. The method of Claim 1, wherein the source and drain regions are doped
- 2 oppositely to said channel region.
- 1 6. The method of Claim 1, wherein the source and drain regions are
- 2 interchangeable.

1 7. The method of Claim 1, wherein step of forming the gate electrode layer
2 includes covering the entire portion of the dielectric layer in the channel region.

1 8. The method of Claim 2, wherein step of forming the gate electrode layer
2 includes covering the entire portion of the dielectric layer in the channel region.

1 9. The method of Claim 1, wherein step of forming the gate electrode layer
2 includes forming the gate electrode layer peripherally about the dielectric layer and covering
3 the portion of the dielectric layer in the channel region.

1 10. A metal oxide semiconductor field effect transistor (MOSFET) having a
2 substrate, comprising:

3 spaced apart source and drain regions on the substrate with the space between
4 the source and drain regions defining a channel region;

5 a dielectric layer peripherally about the drain region to completely surround the
6 drain region and filling the channel region such that the dielectric layer is in contact with the
7 source region, wherein the area of the dielectric layer in the channel region between the drain
8 and source regions is variable in length; and,

9 a gate electrode layer covering at least a portion of the dielectric layer in the
10 channel region.

1 11. The MOSFET of Claim 10, wherein the substrate is a layer of mono-
2 crystalline silicon, the dielectric layer is silicon dioxide and the gate electrode layer is poly-
3 crystalline silicon.

1 12. The MOSFET of Claim 10, wherein a width-length ratio of the transistor
2 is less than or equal to unity.

1 13. The MOSFET of Claim 11, wherein a width-length ratio of the transistor
2 is less than or equal to unity.

1 14. The MOSFET of Claim 10, wherein the source and drain regions are
2 doped oppositely to a channel region.

1 15. The MOSFET of Claim 10, wherein said source and drain regions are
2 interchangeable.

1 16. The MOSFET of Claim 10, wherein the gate electrode layer covers the
2 portion of the dielectric layer in the channel region.

1 17. The MOSFET of Claim 11, wherein the gate electrode layer covers the
2 portion of the dielectric layer in the channel region.

1 18. The MOSFET of Claim 10, wherein the gate electrode layer is peripherally
2 about the dielectric layer and covers the portion of the dielectric layer in the channel region.